IN THE SPECIFICATION

Please amend the Brief Description of the Drawings as follows:

FIG. 1 is a block diagram of the architecture of a parallel pattern detection engine (PPDE) according to embodiments of the present invention comprising N processing units;

FIG. 2A-2D are block diagrams of four matching modes which may be programmed for each of the N processing units (PUs) of FIG. 1;

FIG. 3 is a chart illustrating the various modes of scalability of the PPDE of the present invention;

FIG. 4 is a chart of performance results achievable by an integrated circuit employing 1500 PUs according to embodiments of the present invention;

FIG. 5 is an overview block diagram of an individual PU according to embodiments of the present invention;

FIG. 6 is a detailed block diagram of an individual PU according to embodiments of the present invention;

FIG. 7 is a detailed block diagram of a PU architecture;

FIG. 8 is a circuit diagram of a specific implementation of a single PU;

FIG. 9 is a flow diagram of method steps in embodiments of the present invention;

FIG. 10 is a data processing system suitable for practicing embodiments of the present invention;

FIG. ~~11A-11E~~ 11A-11G illustrate operation in various modes of pattern matching according to embodiments of the present invention;

FIG. 12 is a circuit block diagram of cascading circuitry used for communication between multiple PU 500 units within a PPDE 100 according to embodiments of the present invention; and

FIG. 13 is another block diagram of the communication circuitry between a PU 500 and two adjacent PU 500 units according to embodiments of the present invention.

Please amend the paragraph beginning on page 17, line 1 as follows:

FIGS. ~~11A-11F~~ 11A-11G illustrate actions taken relative to a pattern 601 when comparing to an input data stream 750. FIG. 11A illustrates three clock cycles of the case 1100 where input data 750 is "AAC" being compared to pattern data 601 as "ABC" where each pattern byte has an Opcode 602. The actions 1101 are taken in response to the Opcodes 602. In clock cycle 1, pointer 614 starts at the byte ("A") in pattern 601. The first byte of input data 750 is also an "A". Opcode 602 for the first byte in pattern 601 is set to "match". Since the first byte of input data 750 and pattern 601 compare and Opcode 601 is set to "match", the pointer is incremented moving to the second byte in pattern 601 which is a "B". This happens in one clock cycle, therefore, in the second clock cycle (labeled 1102 because it is significant to the particular pattern in FIG. 11A), the second byte in input pattern 750 ("A") is compared to the second byte in pattern 601 ("B"). The Opcode 602 for the second byte of pattern 602 is set to "match". Since these two bytes do not compare, the sequence "AB" in pattern 601 cannot match the first two bytes "AA" of input data 750 as required by the Opcode 602. Therefore, in clock cycle 2 (1102), pointer 614 is reloaded with the address of the first byte in pattern 602 and comparison begins again. In clock cycle 3, the third byte in input data 750 is compared to the first "A" in pattern 602.